PATENT
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UNITED STATES PATENT APPLICATION

OF

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FOR

INTEGRAL VERTICAL CAVITY SURFACE EMITTING LASER AND POWER MONITOR

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CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] Not Applicable.

BACKGROUND OF THE INVENTION

Field of the Invention

[0002] This invention relates to vertical cavity surface emitting lasers. More specifically, it relates to vertical cavity surface emitting lasers having integrally packaged power monitors.

Discussion of the Related Art

[0003] Vertical cavity surface emitting lasers (VCSELs) represent a relatively new class of semiconductor lasers. While there are many variations of VCSELs, one common characteristic is that they emit light perpendicular to a wafer surface. VCSELs can be formed from a wide range of material systems to produce specific characteristics. VCSELs typically have active regions, distributed Bragg reflector (DBR) mirrors, current confinement structures, substrates, and contacts. Because of their complicated structure and because of their material requirements, VCSELs are usually grown using metal-organic chemical vapor deposition (MOCVD) or molecular beam epitaxy (MBE).

[0004] Figure 1 illustrates a typical VCSEL 10. As shown, an n-doped gallium arsenide (GaAS) substrate 12 is disposed with an n-type electrical contact 14. An n-doped lower mirror stack 16 (a DBR) is on the GaAS substrate 12, and an n-type graded-index lower spacer 18 is disposed over the lower mirror stack 16. An active

region 20 with quantum wells is formed over the lower spacer 18. A p-type graded-index top spacer 22 is disposed over the active region 20, and a p-type top mirror stack 24 (another DBR) is disposed over the top spacer 22. Over the top mirror stack 24 is a p-conduction layer 9, a p-type GaAs cap layer 8, and a p-type electrical contact 26.

[0005] Still referring to Figure 1, the lower spacer 18 and the top spacer 22 separate the lower mirror stack 16 from the top mirror stack 24 such that an optical cavity is formed. As the optical cavity is resonant at specific wavelengths, the mirror separation is controlled to resonant at a predetermined wavelength (or at a multiple thereof). At least part of the top mirror stack 24 includes an insulating region 40 that is formed by implanting protons into the top mirror stack 24 or by forming an oxide layer. The insulating region 40 has a conductive annular central opening 42. Thus, the central opening 42 forms an electrically conductive path though the insulating region 40.

[0006] In operation, an external bias causes an electrical current 21 to flow from the p-type electrical contact 26 toward the n-type electrical contact 14. The insulating region 40 and the conductive central opening 42 confine the current 21 flow through the active region 20. Some of the electrons in the current 21 are converted into photons in the active region 20. Those photons bounce back and forth (resonate) between the lower mirror stack 16 and the top mirror stack 24. While the lower mirror stack 16 and the top mirror stack 24 are very good reflectors, some of the photons leak out as light 23 that travels along an optical path. Still referring to Figure 1, the light 23 passes through the p-type conduction layer 9, through the p-type

GaAs cap layer 8, through an aperture 30 in the p-type electrical contact 26, and out of the surface of the vertical cavity surface emitting laser 10.

[0007] It should be understood that Figure 1 illustrates a typical VCSEL, and that numerous variations are possible. For example, the dopings can be changed (say, providing a p-type substrate), different material systems can be used, operational details can be varied, and additional structures, such as tunnel junctions, can be added.

[0008] While generally successful, VCSELs have are not without problems. For example, it is sometimes important to control the optical power out of a VCSEL. In many applications the desired optical power output is the highest value possible, consistent with eye safety and reliability. Ideally, the desired optical power output is achieved despite manufacturing variances and tolerances, temperature effects, and aging. It is known to sense the optical power output and to use electronic circuitry to control that output. Ideally, a VCSEL and an output power sensor are designed to work together efficiently. One way of doing this is illustrated in United States Patent 6,069,905. That patent discloses a mirror-based laser intensity control system in which a VCSEL and an output power sensor are situated on one substrate. However, at least because of the mirror, that technique might not be optimal.

[0009] Therefore, a new technique of integrating a VCSEL and an output power sensor would be beneficial. Even more beneficial would be a technique in which an output power sensor is directly aligned with a VCSEL. Still more beneficial would be a technique of integrally packaging an output power sensor and a VCSEL such that those elements are optically aligned.

SUMMARY OF THE INVENTION

[00010] The following summary of the invention is provided to facilitate an understanding of some of the innovative features unique to the present invention, and is not intended to be a full description. A full appreciation of the various aspects of the invention can be gained by taking the entire specification, claims, drawings, and abstract as a whole.

[00011] Accordingly, the principles of the present invention are directed to an integrally packaged VCSEL and output power sensor that substantially obviates one or more limitations and/or disadvantages of the related art. According to the principles of the present invention, a VCSEL and an output power sensor are integrally packaged on a substrate such that the VCSEL and the output power sensor are optically aligned.

[0010] An assembly according to the principles of the present invention includes a silicon substrate having a cavity. A VCSEL is mounted on that silicon substrate and aligned such that light from the VCSEL travels along a light path that passes through the cavity, and an optical power sensor formed on the silicon substrate and disposed in the light path. Beneficially, the optical power sensor is a metal-semiconductor-metal photodetector in which the silicon substrate forms the semiconductor. However, other semiconductor photodetection devices, such as photoconductors or pn-junction photodiodes, are also suitable for use in the current invention.) Therefore, the silicon substrate is beneficially doped. Also beneficially, the silicon substrate cavity is formed by anisotropic etching.

[0011] An assembly according to the principles of the present invention can include an optical element (such as a lens) disposed in the cavity and in the light path. Furthermore, that optical element beneficially couples light from the VCSEL into an optical fiber. A compound, such as an epoxy adhesive, fills at least part of the cavity so as to retain the optical element and an end of the optical fiber in the cavity.

[0012] The novel features of the present invention will become apparent to those of skill in the art upon examination of the following detailed description of the invention or can be learned by practice of the present invention. It should be understood, however, that the detailed description of the invention and the specific examples presented, while indicating certain embodiments of the present invention, are provided for illustration purposes only because various changes and modifications within the spirit and scope of the invention will become apparent to those of skill in the art from the detailed description of the invention and claims that follow.

BRIEF DESCRIPTION OF THE DRAWING

[0013] The accompanying figures, in which like reference numerals refer to identical or functionally-similar elements throughout the separate views and which are incorporated in and form part of the specification, further illustrate the present invention and, together with the detailed description of the invention, serve to explain the principles of the present invention.

[0014] In the drawings:

[0015] Figure 1 illustrates a typical vertical cavity surface emitting laser;

[0016] Figure 2 illustrates a sectional view of an integrally packaged VCSEL and optical power sensor assembly according to the principles of the present invention;

[0017] Figure 3 illustrates controlling the optical power sensor of the VCSEL illustrated in Figure 2;

[0018] Figure 4 illustrates a sectional view of a portion of an n-type silicon <100> substrate used in the integrated VCSEL and optical power sensor assembly illustrated in Figure 2, during the fabrication of that assembly;

[0019] Figure 5 illustrates the silicon substrate of Figure 4 after anisotropic etching; and

[0020] Figure 6 illustrates the silicon substrate of Figure 5 after contact ring formation, and after an optional reactive ion etching of the silicon substrate.

[0021] Note that in the drawings that like numbers designate like elements. Additionally, for explanatory convenience the descriptions use directional signals such as up and down, top and bottom, and lower and upper. Such signals, which are derived from the relative positions of the elements illustrated in the drawings, are meant to aid the understanding of the present invention, not to limit it.

DETAILED DESCRIPTION OF THE ILLUSTRATED EMBODIMENTS

[0022] Reference will now be made in detail to an embodiment of the present invention, example of which is illustrated in the accompanying drawings.

[0023] The principles of the present invention provide for integrally packaged VCSEL and optical power sensor assemblies. An example of such an assembly is the VCSEL and optical power sensor assembly 110 illustrated in Figure 2. That assembly

110 includes a VCSEL 112 that emits light 114 through an optical power sensor 116. Both the VCSEL 112 and the optical power sensor 116 are on a semiconductor substrate 118. The VCSEL 112 is attached to the semiconductor substrate 118 by a metallic ring or pads 120, which is/are deposited on the semiconductor substrate 118, and by solder bumps 122. The solder bumps 122 contact the bottom of the VCSEL 112, which includes metallic contacts. The top of the VCSEL 112 optionally includes a contact 113 to which a lead 115 is attached.

[0024] The optical power sensor 116 is beneficially a metal-semiconductor-metal photodetector that is fabricated on the silicon substrate 118. Also fabricated on the silicon substrate 118 are contacts 126 for detector leads 128, and a contact 130 for a VCSEL lead 132. The silicon substrate 118 also includes conductive traces that connect the contacts 126 to the optical power sensor 116, and that connect the contact 130 to the ring 120. In another configuration two separate contacts for the VCSEL are fabricated on a single surface. In that configuration the contact 113 and the wire 115 are replaced by traces on the silicon substrate and by separated solder bumps 122.

[0025] Still referring to Figure 2, the silicon substrate 118 includes a cone shaped cavity 136 having inwardly sloping walls that are narrower at the top and broader at the bottom. In the cavity 136 is an optional an optical element 138, which is beneficially a micro-optic lens, and the end portion of an optical fiber 140. Figure 2 illustrates an optional thin silicon membrane 137 between the optical power sensor 116 and the optical element 138. In some applications that membrane is either completely or partially removed. A sealing compound 142, beneficially an epoxy

material, retains the optical element 138 and the end portion of the optical fiber 140 within the cavity 136.

[0026] The operation of the VCSEL and optical power sensor assembly 10 will be explained with the assistance of Figures 2 and 3. A controller 150 receives information from the optical power sensor 116 via leads 128. The controller 150 then compares that information with predetermined information to determine whether the VCSEL is producing light 114 with a predetermined optical power. The information from the optical power sensor 116 depends on the light 114 that irradiates the optical power sensor 116. If the information from the optical power sensor 116 shows that the VCSEL is not producing enough power output, the current through the VCSEL is increased using current on lines 132 and 115 (via the contacts 130 and 113, and the ring 120 and the solder bump 122). Since the optical power sensor 116 absorbs and blocks only part of the light 114, the remaining light 114 is collected by the optical element 138 and coupled into the optical fiber 140.

[0027] A suitable method for fabricating the silicon substrate and its cavity is illustrated in Figures 4, 5, and 6. Referring now to Figure 4, that method begins with the procurement of a silicon <100> substrate 118, say about 400 microns thick. That substrate is then doped to form an N-type body 154 having a thin P/P^+-type layer 156 at its surface.

[0028] Next, referring now to Figure 5, the ring 120, the contacts 126 and 130, a metal layer 160 for the optical power sensor 116, and the electrical interconnects are then formed on the silicon substrate using standard semiconductor fabrication techniques.

[0029] Referring now to Figure 6, the bottom of the silicon substrate is then protected with an etch protector (such as silicon nitride), and an opening through that etch protector is formed at the desired location, again using standard photolithographic techniques. The opening exposes an area of the silicon substrate to chemical action. The exposed area is then anisotropically etched (using a suitable etchant such as potassium hydroxide). The anisotropic etching proceeds along crystalline planes at inwardly sloping angles so that the resulting cavity is wider at its bottom then at its top. Etching is stopped when a thin membrane 137 (see Figure 2) is formed. If the membrane 137 is to remain in place, the fabrication of the silicon substrate 118 stops. Alternatively, the membrane can be reactive ion etched to form an opening 121 from the cavity through the silicon substrate 118. This improves light transmission through from the VCSEL 112 to the optical fiber 140 (see Figure 2). The etch protector is then removed. An optional final step would be to coat the bottom of the membrane with a thin, partially transparent material such as a metal film. This provides the opportunity to reduce the transmission from the VCSEL through the detector 116 and membrane 137, should that be desired.

[0030] With the silicon substrate complete the VCSEL and leads 132 and 128 are soldered to the ring 120 and contacts 130 and 126. Then, the lead 115 is soldered to the contact 113. The resulting structure is then inverted and the optical element 138 is placed in the cavity 136. An end portion of the optical fiber 140 is then located in position adjacent the optical element 130. With standard lithographic and manufacturing techniques, the entire assembly is self-aligning. The VCSEL aligns to the detector 116 and the cavity 136 thorough surface tension of the attachment solder

122. Additionally, the fiber 140 and the optional optical element 138 align to the cavity 136 through the interference with the sloping sidewalls. The cavity is then filled with a sealant 142 (beneficially an epoxy). After the sealant hardens, the resulting integral assembly can be located on a PC board (via rings 170 formed on the silicon substrate 118, reference Figure 6) or packaged in a carrier (not shown).

[0031] The embodiments and examples set forth herein are presented to best explain the present invention and its practical application and to thereby enable those skilled in the art to make and utilize the invention. Those skilled in the art, however, will recognize that the foregoing description and examples have been presented for the purpose of illustration and example only. Other variations and modifications of the present invention will be apparent to those of skill in the art, and it is the intent of the appended claims that such variations and modifications be covered. The description as set forth is not intended to be exhaustive or to limit the scope of the invention. Many modifications and variations are possible in light of the above teaching without departing from the spirit and scope of the following claims. It is contemplated that the use of the present invention can involve components having different characteristics. It is intended that the scope of the present invention be defined by the claims appended hereto, giving full cognizance to equivalents in all respects.